



quantumdata

980 MHL CBUS COMPLIANCE MODULE

Now approved by MHL Consortium!

The MHL CBUS Compliance module enables you to conduct compliance tests on your MHL devices—sources, sinks and dongles—using an MHL-approved test instrument in accordance with the MHL Compliance Test Specifications (CTS) 1.2, 1.3, 2.0 and 2.1. The module provides complete test coverage of the CBUS Link Layer tests, RCP tests and Common tests.

The 980 MHL CBUS Compliance Test module can be equipped in either of the Quantum Data Advanced Test Platforms:

- 980 - 2-slot, 10.4" touch display
- 980B - 5-slot, 15" touch display.

The 980's suite of compliance test applications are an ideal solution for pre-testing or self-testing (where permitted) your MHL devices as they enable you to get your MHL product to market more quickly and to reduce or avoid the expense of testing or re-testing at the Authorized Testing Centers (ATCs).

The 980 MHL CBUS Compliance module's tests can be controlled either through the embedded 980 GUI Manager running on the 980 platform itself or the PC-based 980 GUI Manager. The 980 or 980B's built-in color touch screen provides a graphical user interface (GUI) to control the module and run the compliance test.

Detailed test reports and graphical CBUS event Log Plots are provided to help you diagnose Compliance test failures.



980 Advanced Test Platform – CBUS Compliance Module

MHL CBUS COMPLIANCE BENEFITS

Pre-Testing prior to submission to ATC

Run compliance tests on source, sink and dongle devices prior to submission to the ATC for final testing. This reduces the cost and time of having to resubmit if a failure occurs.

Self-Testing

Self-test your MHL device for compliance (when permitted) in your own lab to eliminate the cost and time associated with submitting your product to the ATCs.

No External Test Equipment Required

All tests including compliance tests for physical layer parameters can be performed with the CBUS compliance test module.

Operational Efficiency

Solution offers flexibility in running the tests by enabling you to select a small set of tests to run initially. You can save test configurations and recall them for later use to target specific compliance tests.

Root Cause Identification

When compliance test failures occur, you can view the details of the failure. This enables you to quickly identify the root cause of a compliance test failure.

Data Portability

Data portability enables you to share the test results and log data with colleagues, subject matter experts at other corporate locations and other experts for analysis and for verifying compliance. The 980 test instrument is not required to view the test results. The test reports and graphical event Log Plots can be viewed through the 980 GUI Manager which is free and available from the Quantum Data website.

MHL CBUS BUNDLING OPTIONS

MHL CBUS Source Test

Purchase the MHL CBUS source compliance test suite.

MHL CBUS Sink/Dongle Tests

Purchase the MHL CBUS sink and dongle combination compliance test suite.

MHL CBUS Source and Sink/Dongle Tests

Purchase all MHL CBUS tests, i.e. source and sink/dongle compliance test suites.

MHL Source Protocol Compliance Test & CBUS Source Test

Purchase the MHL Source Protocol compliance test suite (supported on HDMI Protocol Analyzer module) with the MHL CBUS source compliance test suite.

MHL Sink/Dongle Protocol Compliance Test Controller & CBUS Sink/Dongle Test suite

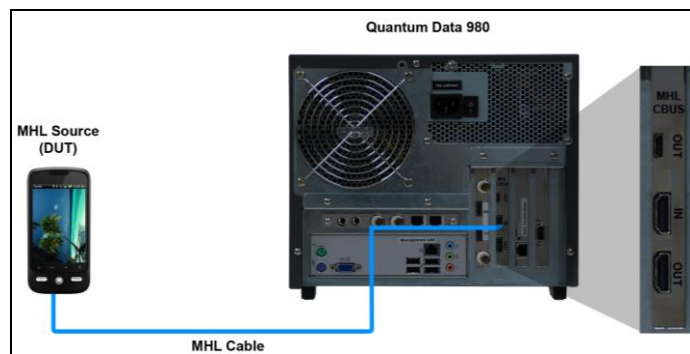
Purchase the MHL Sink/Dongle Protocol Compliance Test Controller (supported on HDMI Protocol Analyzer module and requires the 882EA) with the MHL CBUS sink/dongle compliance test suite.

Rev. A8 – 07/19/2013

MHL CBUS SOURCE COMPLIANCE TESTING

Operational workflow is simple:

1. Connect source device under test to 980.
2. Launch 980 GUI Manager.
3. Complete Capabilities Declaration Form (CDF).
4. Select the tests to run.
5. Review test suite and select options.
6. Initiate test series.
7. View Results.



Event Plot HDMI Src CT 1.4b CBUS Src CT 2.0

CDF Entry Test Selection Test Options / Preview

Open New Save CDF File: <not saved>

General Registers RCP Rcv RCP Send RCP LD Map UCP Rcv (2.0) UCP Send (2.0) 3D Video (2.0)

CDF_CTS_VERSION	CTS Version to test against. 1.2 2.0
CDF_MFR_NAME	What is the product manufacturer's name? Acme
CDF_MODEL_NUMBER	What is the model name/number of the product? XYZ
CDF_SRC_POWERED	Can the Source drive the VBUS? Yes No
CDF_SRC_CBUS_THRESHOLD_V	Voltage at which CBUS Timing Measurements should be taken. This voltage should be halfway between the HIGH and LOW CBUS voltages for data driven by this device. This will be related to the device's VOH. 0.90 V (0.75 to 1.05)
CDF_PROC_SET_ACTIVE	Set Device into Active Mode for Discovery Tests. Edit Procedure
CDF_PROC_SET_STANDBY	Set Device into Standby-Discover Mode. Edit Procedure

Capabilities Declaration Form (CDF) Registers page

Event Plot MHL Src CT 2.0 CBUS Src CT 2.0

CDF Entry Test Selection Test Options / Preview

Open Save Select All Tests Deselect All Tests

Source (3/41) Common (0/67) EDID/Registers (0/2) RCP (0/2) 3D (0/1) UCP (0/2)

3.1.1	TMDS Electrical Tests	0/1	
3.3.3	Link Layer Electrical: Absolute Maximum Voltages	2/2	
3.3.4	Link Layer Timing - DUT Output: Pre-Discovery	0/1	
3.3.5	Link Layer Electrical - DUT Output: Discovery	3/5	
3.3.6	Link Layer Timing - DUT Output: Discovery	0/4	
3.3.7	Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling	0/5	
3.3.8	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds	0/2	
3.3.9	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times	1/2	
3.3.10	Link Layer Timing - DUT Output: Link-Level NACK	0/1	
3.3.11	Link Layer Timing - DUT Output: ACK	0/2	
3.3.12	Link Layer Timing - DUT Output: Bus Re-Arbitration	1/3	
3.3.13	Link Layer Behavior - DUT Output: Ill-formed packets	2/2	
3.3.14	Link Layer Timing - DUT Input: Discovery	0/3	
3.3.15	Link Layer Electrical - DUT Input: Arbitration/Sync/Data signaling	0/1	
3.3.16	Link Layer Timing - DUT Input: Arbitration	0/2	
3.3.17	Link Layer Timing - DUT Input: Data	0/1	
3.3.18	Link Layer Timing - DUT Input: NACK	0/1	
3.3.19	Link Layer Timing - DUT Input: ACK	0/1	
3.3.20	Link Layer Timing - DUT Input: Bus Re-Arbitration	0/1	
3.3.21	Link Layer Behavior - DUT Input: Ill-formed packets	0/1	
3.3.22	Link Layer Timing - DUT Input: Disconnect	0/3	
3.3.23	Link Layer Electrical - DUT VBUS Control	0/3	

3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device
Verify correct Source DUT behavior when going from unplugged to Z(CBUS_SINK_DISCOVER) within the MHL range.

3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL device
Verify correct Source DUT behavior when Sink HIGH-Z's the CBUS to invoke a new (second or subsequent) CBUS Discovery, then attaches with Z(CBUS_SINK_DISCOVER) within the MHL range.

3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage
Verify that Source DUT Pull-up Voltage has correct value when connecting Z(CBUS_SINK_DISCOVER).

Test Selections showing source test selections

Event Plot MHL Src CT 2.0 CBUS Src CT 2.0

CDF Entry Test Selection Test Options / Preview

Instrument: My980 [192.168.254.163]

Test List

Category / Test Name	Status
3.2.6: EDID and Device Capability Register Test	Pass
3.2.6.1: EDID Reading Test	Pass
3.2.6.2: Device Capability Registers Test	Pass
3.2.9: 3D Test	Pass
3.2.9.1: 3D Video Mode Support (3D REQ)	Pass
3.2.10: UCP Sub-Command Tests	Pass
3.2.10.1: UCP Sub-Commands Receiving Test	Pass
3.2.10.2: UCP Sub-Commands Transmitting Test	Fail
3.3.3: Link Layer Electrical: Absolute Maximum Voltages	Pass
3.3.3.2: CBE-Source: VBUS Absolute Maximum Positive Voltage	Pass
3.3.3.3: CBE-Source: CBUS Absolute Maximum Positive Voltage	Pass
3.3.5: Link Layer Electrical - DUT Output: Discovery	Pass
3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device	Fail
3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL device	Pass
3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage	Pass
3.3.9: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times	Pass
3.3.9.2: CBT-Source: Continuous Monitor: Bit Timing Variation within a Packet	Pass
3.3.12: Link Layer Timing - DUT Output: Bus Re-Arbitration	Pass
3.3.12.3: CBT-Source: Source Never Sends Too Many Back-to-Back Packets	Pass
3.3.13: Link Layer Behavior - DUT Output: Ill-formed packets	Pass
3.3.13.1: CBT-Source: Source Never Sends Impulse Noise	Pass
3.3.13.2: CBT-Source: Source Never Sends Partial Packets	Pass
3.3.13.3: CBT-Source: Source Never Sends Partial Packets	Pass
6.3.1: MSC - DUT Input: Device Register Space Contents; Reads	Pass
6.3.1.1: CBM: Capability Regs; READ DEVCAP of Capability Register Contents	Pass
6.3.2: MSC - DUT Output: Vendor-specific and Reserved Header Values	Pass
6.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Values	Pass
6.3.3: MSC - DUT Output: Normal Commands	Pass
6.3.3.1: CBM: DUT sends (0x62) GET STATE command	Pass
6.3.3.2: CBM: DUT sends (0x63) GET VENDOR ID Command	Pass
3.3.13.2: CBT-Source: Source Never Sends Partial Packets	Pass

MHL Source Compliance Test Preview

Event Plot Edit Editor EDID CT 1.4s CBUS Sink CT 1.2 CBUS Sink CT 1.2 CBUS Dongle CT 1.2 CT Results

CBUS Src Compliance Test Results

Results Name: Acme_MHL_Tests Manufacturer: Acme

Date Tested: October 2, 2012 2:05 PM Model Name: XYZ

Overall Status: CTS 1.2 - Incomplete Port Tested: 1

Test Name / Details	Status
3.3.3.2: CBE-Source: VBUS Absolute Maximum Positive Voltage	Pass
3.3.3.3: CBE-Source: CBUS Absolute Maximum Positive Voltage	Pass
3.3.4.1: CBT-Source: Time from Source VBUS Application to Disc	Fail
3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device	Incomplete
3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL dev	Pass
3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage	Incomplete
3.3.5.4: CBE-Source: Discovery Pulse Drive HIGH Voltage	Pass
3.3.5.5: CBE-Source: Discovery Pulse Float LOW Voltage	Pass
3.3.9.2: CBT-Source: Continuous Monitor: Bit Timing Variation	Pass
3.3.12.3: CBT-Source: Source Never Sends Too Many Back-to-Back	Pass
3.3.13.1: CBT-Source: Source Never Sends Impulse Noise	Pass
3.3.13.2: CBT-Source: Source Never Sends Partial Packets	Pass
3.3.14.1: CBT-Source: Discovery: Sink Responds Correctly; Time	Fail
01: dUT discovered in 3370 ms.	Pass
02: dUT does switch its pull-up from ZCBUS_SRC_DISCOVER to	Pass
3.3.14.2: CBT-Source: Discovery: Sink Responds Late	Incomplete
3.3.14.3: CBT-Source: Discovery: Sink Never Drives MHL+/- HIGH	Pass
3.3.22.1: CBT-Source: Remove MHL+/- Pull-ups for Less than Gli	Pass
3.3.22.2: CBT-Source: Remove MHL+/- Pull-up for More than Gli	Pass
3.3.22.3: CBT-Source: Time from Disconnect until VOUT Falls	Fail
6.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Va	Pass
6.3.3.1: CBM: DUT sends (0x62) GET STATE command	Pass
6.3.3.2: CBM: DUT sends (0x63) GET VENDOR ID Command	Pass

3.2.6.1: EDID Reading Test

Instrument: My980 [192.168.254.135]

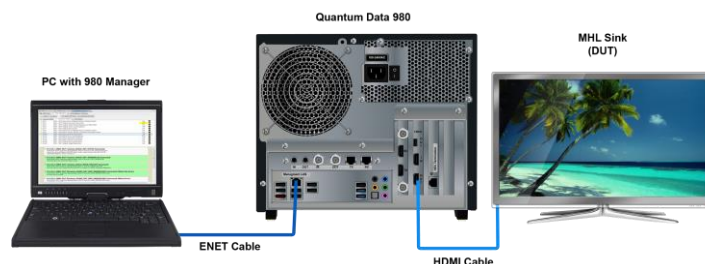
Continue Test Execution

MHL Source Compliance Test Results

MHL CBUS SINK COMPLIANCE TESTING

Operational workflow is simple:

1. Connect sinkdevice under test to 980.
2. Launch 980 GUI Manager.
3. Complete Capabilities Declaration Form (CDF).
4. Select the tests to run.
5. Review test suite and select options.
6. Initiate test series.
7. View Results.



Capabilities Declaration Form (CDF) RCP page

Test Selections showing sink test selections

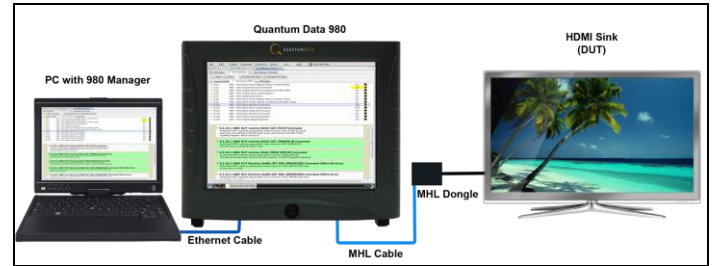
MHL Sink Compliance Test Preview

MHL Sink Compliance Test Results

MHL CBUS DONGLE COMPLIANCE TESTING

Operational workflow is simple:

1. Connect dongle device under test to 980.
2. Launch 980 GUI Manager.
3. Complete Capabilities Declaration Form (CDF).
4. Select the tests to run.
5. Review test suite and select options.
6. Initiate test series.
7. View Results.



Capabilities Declaration Form (CDF) RCP page

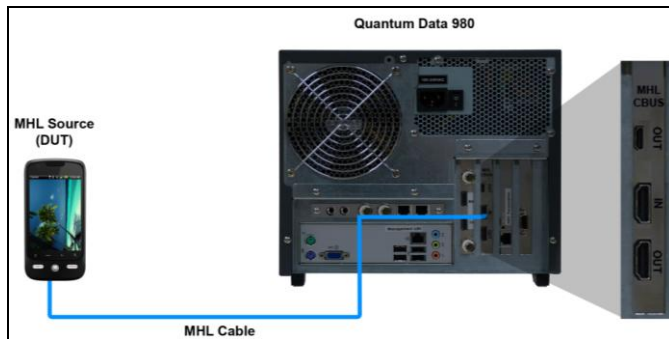
Test Selections showing dongle test selections

MHL Dongle Compliance Test Preview

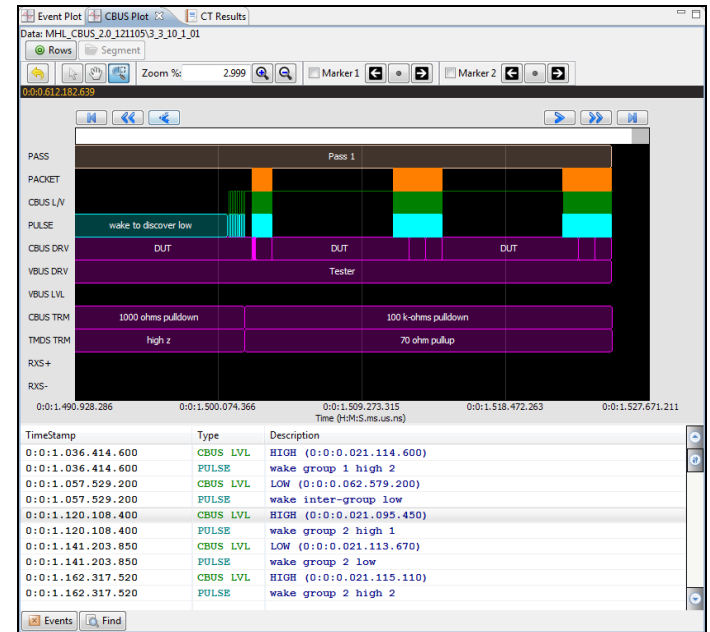
MHL Dongle Compliance Test Results

MHL CBUS EVENT LOG PLOTS

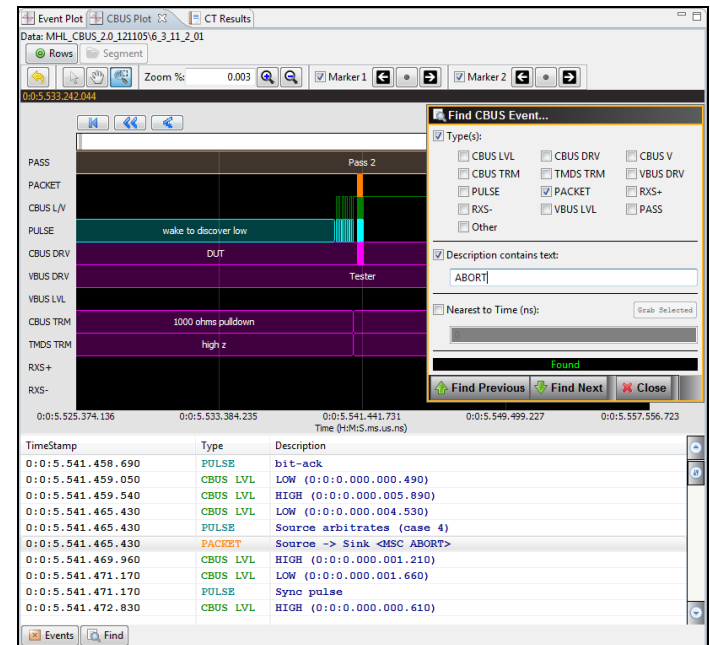
Provides graphical view of CBUS events:



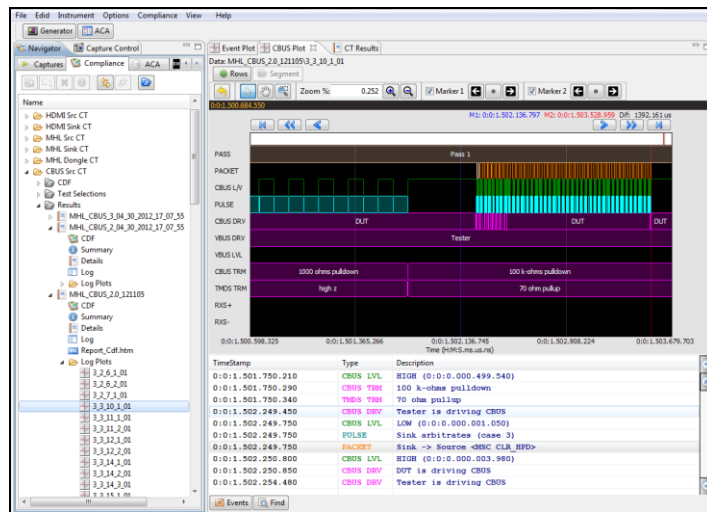
CBUS Source Test Setup (example)



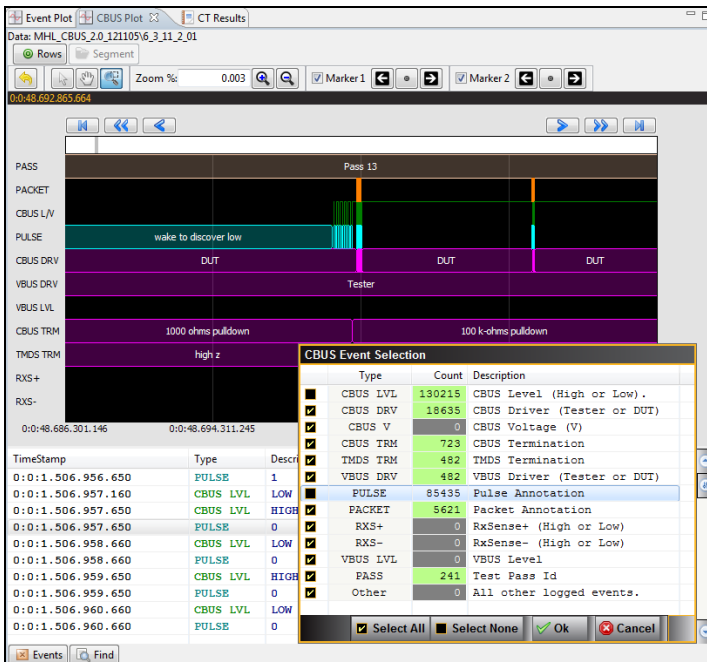
CBUS Log Plots (Source test example)



CBUS Log Plots (Searching for Events)



CBUS Log Plots Accessed via Navigator/Compliance Panel (right)



CBUS Log Plots (Filtering Events)

MHL CBUS SOURCE COMPLIANCE TESTS

This module supports CBUS compliance testing of MHL source devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

3 Source Test**3.1 Electrical Test**

3.1.1.13 Rx Sense Impedance

3.2 System Test

3.2.6 EDID and Device Capability Register Test

3.2.6.1 EDID Reading Test

3.2.6.2 Device Capability Registers Test (Available for MHL CTS 1.3, 2.0, 2.1)

3.2.7 RCP Sub-Command Tests

3.2.9 3D Video Tests (Available for MHL CTS 2.0, 2.1)

3.2.9.1 3D Video Mode Support (3D Req)

3.2.10 UCP Sub-Command Tests (Available for MHL CTS 2.0, 2.1)

3.3 CBUS Tests (all tests)

3.3.3 Link Layer Electrical – Source: Absolute Maximum Voltages

3.3.4 Link Layer Timing – Source DUT Output: Pre-Discovery

3.3.5 Link Layer Electrical – Source DUT Output: Discovery

3.3.6 Link Layer Timing – Source DUT Output: Discovery

3.3.7 Link Layer Electrical – Source DUT Output: Arbitration/Sync/Data Signaling

3.3.8 Link Layer Timing – Source DUT Output: Arbitration/Sync/Data in Nanoseconds

3.3.9 Link Layer Timing – Source DUT Output: Arbitration/Sync/Data in Bit Times

3.3.10 Link Layer Timing – Source DUT Output: Link-Level NACK

3.3.11 Link Layer Timing – Source DUT Output: ACK

3.3.12 Link Layer Timing – Source DUT Output: Bus Re-Arbitration

3.3.13 Link Layer Behavior – Source DUT Output: Ill-formed packets

3.3.14 Link Layer Timing – Source DUT Input: Discovery

3.3.15 Link Layer Electrical – Source DUT Input: Arbitration/Sync/Data signaling

3.3.16 Link Layer Timing – Source DUT Input: Arbitration

3.3.17 Link Layer Timing – Source DUT Input: Data

3.3.18 Link Layer Timing – Source DUT Input: NACK

3.3.19 Link Layer Timing – Source DUT Input: ACK

3.3.20 Link Layer Timing – Source DUT Input: Bus Re-Arbitration

3.3.21 Link Layer Behavior – Source DUT Input: Ill-formed packets

3.3.22 Link Layer Timing – Source DUT Input: Disconnect

3.3.23 Link Layer Electrical – Source DUT VBUS Control

MHL CTS Source tests supported by 980 HDMI Protocol Analyzer Module:

3.2.2 TMDS Encoding

3.2.2.1 Legal Codes

3.2.2.2 Basic Protocol

3.2.2.3 Packet Types

3.2.3 Video Modes

3.2.3.1 Video Formats

3.2.3.2 Pixel Encodings

3.2.3.3 AVI Infoframe

3.2.3.4 Video Quantization Ranges

3.2.4 Audio Tests

3.2.4.1 IEC 60958 / IEC 61937

3.2.4.2 Audio Clock Regeneration

3.2.4.3 Audio Infoframes

3.2.5 EDID and Device Capability Register Test

3.2.5.1 Device Status Registers Test (Available for MHL CTS 2.0)

3.2.6 EDID and Device Capability Register Test

3.2.6.3 Device Status Registers Test (Available for MHL CTS 1.3, 2.0, 2.1)

3.2.8 RAP Sub-Command Tests (Available for MHL CTS 1.3, 2.0, 2.1)

3.2.9 3D Video Tests (Available for MHL CTS 2.0, 2.1)

3.2.9.2 3D Video Format Timings (Available for MHL CTS 2.0, 2.1)

3.2.9.3 3D Video Mode Indicator (Available for MHL CTS 2.0, 2.1)

MHL Source tests supported by 882EA Video Test Instrument:

3.2.5 HDCP Test

MHL CBUS SINK COMPLIANCE TESTS

This module supports CBUS compliance testing of MHL sink devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

4 MHL Sink Test**4.1 Electrical Test**

4.1.1.7 Rx Sense Impedance

4.2 MHL System Tests (Requires 882EA except where noted)

4.2.5 EDID and Device Capability Register Test

4.2.5.1 EDID Test

4.2.5.2 Device Capability Registers Test

4.2.5.3 Device Status Registers Test (Available for MHL CTS 1.3, 2.0, 2.1)

4.2.6 RCP Sub-Command Test

4.2.8 3D Video Tests Available for MHL CTS 2.0, 2.1)

4.2.8.1 3D Video Mode Support Data

4.2.9 UCP Sub-Command Test (Available for MHL CTS 2.0, 2.1)

4.3 CBUS Tests (all tests)

4.3.3 Link Layer Electrical – Sink: Absolute Maximum Voltages

4.3.4 Link Layer Electrical – Sink DUT Output: Standby/Discovery Impedance

4.3.5 Link Layer Timing – Sink DUT Output: Pre-Discovery

4.3.6 Link Layer Electrical – Sink DUT Output: Arbitration/Sync/Data Signaling

4.3.7 Link Layer Timing – Sink DUT Output: Arbitration/Sync/Data in Nanoseconds

4.3.8 Link Layer Timing – Sink DUT Output: Arbitration/Sync/Data in Bit Times

4.3.9 Link Layer Timing – Sink DUT Output: Link Level NACK

4.3.10 Link Layer Timing – Sink DUT Output: Link Level ACK

4.3.11 Link Layer Timing – Sink DUT Output: Bus Re-Arbitration

4.3.12 Link Layer Timing – Sink DUT Output: Ill-formed packets

4.3.13 Link Layer Electrical – Sink DUT Input: Discovery

4.3.14 Link Layer Timing – Sink DUT Input: Discovery OK

4.3.15 Link Layer Timing – Sink DUT Input: Discovery Reject

4.3.16 Link Layer Electrical – Sink DUT Input: Arbitration/Sync/Data Signaling

4.3.17 Link Layer Timing – Sink DUT Input: Arbitration

4.3.18 Link Layer Timing – Sink DUT Input: Data

4.3.19 Link Layer Timing – Sink DUT Input: NACK

4.3.20 Link Layer Timing – Sink DUT Input: ACK

4.3.21 Link Layer Timing – Sink DUT Input: Bus Re-Arbitration

4.3.22 Link Layer Timing – Sink DUT Input: Ill-formed Packets

4.3.23 Link Layer Timing – Sink DUT Input: Disconnect

4.3.24 Link Layer Electrical – Sink DUT VBUS Output

4.3.25 Link Layer Timing – Sink DUT VBUS Turn On Transition

MHL CTS Sink tests supported by 980 HDMI Protocol Analyzer Module:**4.2 MHL System Tests (Requires 882EA except where noted)**

4.2.1 TMDS Coding (Requires 882EA except where noted)

4.2.1.1 Character Synchronization (882EA not required)

4.2.1.2 Packet Type

4.2.2 Video Tests (Requires 882EA)

4.2.2.1 Video Format

4.2.2.2 Pixel Encoding

4.2.2.3 Video Quantization Ranges

4.2.3 Audio Test (Requires 882EA)

4.2.3.1 IEC 60958 / IEC 61937

4.2.3.2 Audio Clock Regeneration

4.2.7 RAP Sub-Command Test (Available for MHL CTS 2.0, 2.1)

4.2.8 3D Video Tests (Available for MHL CTS 2.0, 2.1)

4.2.8.2 3D Video Format (Available for MHL CTS 2.0, 2.1)

MHL Sink tests supported by 882EA Video Test Instrument:

4.2.4 HDCP Test

MHL CBUS DONGLE COMPLIANCE TESTS

This module supports CBUS compliance testing of MHL sink devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

5 MHL Dongle Test**5.1 Electrical Test**

- 5.1.1.7 Rx Sense Impedance (Powered)
- 5.1.1.8 Rx Sense Impedance (Unpowered)

5.2 MHL System Tests (Requires 882EA except where noted)

- 5.2.5 EDID and Device Capability Register Test
 - 5.2.5.1 EDID Test
 - 5.2.5.2 Device Capability Registers Test
 - 5.2.5.3 Device Status Registers Test (Available for MHL CTS 1.3.2.0, 2.1)
- 5.2.6 RCP Sub-Command Test
- 5.2.8 3D Video Tests (Available for MHL CTS 2.0, 2.1)
 - 5.2.8.1 3D Video Mode Support Data
- 5.2.9 UCP Sub-Command Test (Available for MHL CTS 2.0, 2.1)

5.3 CBUS Tests (all tests)

- 5.3.3 Link Layer Electrical – Dongle: Absolute Maximum Voltages
- 5.3.4 Link Layer Electrical – Dongle DUT Output: Discovery Impedance
- 5.3.5 Link Layer Timing – Dongle DUT Output: Pre-Discovery
- 5.3.6 Link Layer Electrical – Dongle DUT Output: Arbitration/Sync/Data Signaling
- 5.3.7 Link Layer Timing – Dongle DUT Output: Arbitration/Sync/Data in Nanoseconds
- 5.3.8 Link Layer Timing – Dongle DUT Output: Arbitration/Sync/Data in Bit Times
- 5.3.9 Link Layer Timing – Dongle DUT Output: Link Level NACK
- 5.3.10 Link Layer Timing – Dongle DUT Output: Link Level ACK
- 5.3.11 Link Layer Timing – Dongle DUT Output: Bus Re-Arbitration
- 5.3.12 Link Layer Timing – Dongle DUT Output: Ill-formed packets
- 5.3.13 Link Layer Electrical – Dongle DUT Input: Discovery
- 5.3.14 Link Layer Timing – Dongle DUT Input: Discovery OK
- 5.3.15 Link Layer Timing – Dongle DUT Input: Discovery Reject
- 5.3.16 Link Layer Electrical – Dongle DUT Input: Arbitration/Sync/Data Signaling
- 5.3.17 Link Layer Timing – Dongle DUT Input: Arbitration
- 5.3.18 Link Layer Timing – Dongle DUT Input: Data
- 5.3.19 Link Layer Timing – Dongle DUT Input: NACK
- 5.3.20 Link Layer Timing – Dongle DUT Input: ACK
- 5.3.21 Link Layer Timing – Dongle DUT Input: Bus Re-Arbitration
- 5.3.22 Link Layer Timing – Dongle DUT Input: Ill-formed Packets
- 5.3.23 Link Layer Timing – Dongle DUT Input: Disconnect
- 5.3.24 Link Layer Electrical – Dongle DUT VBUS Output
- 5.3.25 Link Layer Electrical – Dongle DUT VBUS Input
- 5.3.26 Link Layer Timing – Dongle DUT VBUS Transition

MHL CTS Dongle tests supported by 980 HDMI Protocol Analyzer Module:

- 5.2.1 TMDS Coding (Requires 882EA except where noted)
 - 5.2.1.1 Character Synchronization (882EA not required)
 - 5.2.1.2 Packet Type
- 5.2.2 Video Tests (Requires 882EA)
 - 5.2.2.1 Video Format
 - 5.2.2.2 Pixel Encoding
 - 5.2.2.3 Video Quantization Ranges
- 5.2.3 Audio Test (Requires 882EA)
 - 5.2.3.1 IEC 60958 / IEC 61937
 - 5.2.3.2 Audio Clock Regeneration
- 5.2.7 RAP Sub-Command Test (Available for MHL CTS 2.0, 2.1)
- 5.2.8 3D Video Tests (Available for MHL CTS 2.0, 2.1)
 - 5.2.8.2 3D Video Format

MHL Dongle tests supported by 882EA Video Test Instrument:

- 5.2.4 HDCP Test (supported through 882EA)

MHL CBUS COMMON COMPLIANCE TESTS

This module Supports CBUS compliance common tests for MHL Common devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

6 Tests Common to Sources, Sinks, Dongles**6.3 CBUS Tests (all tests)**

- 6.3.1 MSC – Source and Sink DUT Input: Device Register Space Contents; Reads
- 6.3.2 MSC – Source and Sink DUT Output: Vendor Specific and Reserved Header Values
- 6.3.3 MSC – Source and Sink DUT Output: Normal Commands
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