quantumdata

980 MHL CBUS COMPLIANCE MODULE

Now approved by MHL Consortium!

The MHL CBUS Compliance module enables you to conduct compliance tests on your MHL devices—sources, sinks and dongles—using an MHL-approved test instrument in accordance with the MHL Compliance Test Specifications (CTS) 1.2, 1.3, 2.0 and 2.1. The module provides complete test coverage of the CBUS Link Layer tests, RCP tests and Common tests.

The 980 MHL CBUS Compliance Test module can be equipped in either of the Quantum Data Advanced Test Platforms:

- 980 - 2-slot, 10.4" touch display
- 980B - 5-slot, 15" touch display.

The 980's suite of compliance test applications are an ideal solution for pre-testing or self-testing (where permitted) your MHL devices as they enable you to get your MHL product to market more quickly and to reduce or avoid the expense of testing or re-testing at the Authorized Testing Centers (ATCs).

The 980 MHL CBUS Compliance module's tests can be controlled either through the embedded 980 GUI Manager running on the 980 platform itself or the PC-based 980 GUI Manager. The 980 or 980B's built-in color touch screen provides a graphical user interface (GUI) to control the module and run the compliance test.

Detailed test reports and graphical CBUS event Log Plots are provided to help you diagnose Compliance test failures.

980 Advanced Test Platform – CBUS Compliance Module

MHL CBUS COMPLIANCE BENEFITS

Pre-Testing prior to submission to ATC
Run compliance tests on source, sink and dongle devices prior to submission to the ATC for final testing. This reduces the cost and time of having to resubmit if a failure occurs.

Self-Testing
Self-test your MHL device for compliance (when permitted) in your own lab to eliminate the cost and time associated with submitting your product to the ATCs.

No External Test Equipment Required
All tests including compliance tests for physical layer parameters can be performed with the CBUS compliance test module.

Operational Efficiency
Solution offers flexibility in running the tests by enabling you to select a small set of tests to run initially. You can save test configurations and recall them for later use to target specific compliance tests.

Root Cause Identification
When compliance test failures occur, you can view the details of the failure. This enables you to quickly identify the root cause of a compliance test failure.

Data Portability
Data portability enables you to share the test results and log data with colleagues, subject matter experts at other corporate locations and other experts for analysis and for verifying compliance. The 980 test instrument is not required to view the test results. The test reports and graphical event Log Plots can be viewed through the 980 GUI Manager which is free and available from the Quantum Data website.

MHL CBUS BUNDLING OPTIONS

MHL CBUS Source Test
Purchase the MHL CBUS source compliance test suite.

MHL CBUS Sink/Dongle Tests
Purchase the MHL CBUS sink and dongle combination compliance test suite.

MHL CBUS Source and Sink/Dongle Tests
Purchase all MHL CBUS tests, i.e. source and sink/dongle compliance test suites.

MHL Source Protocol Compliance Test & CBUS Source Test
Purchase the MHL Source Protocol compliance test suite (supported on HDMI Protocol Analyzer module) with the MHL CBUS source compliance test suite.

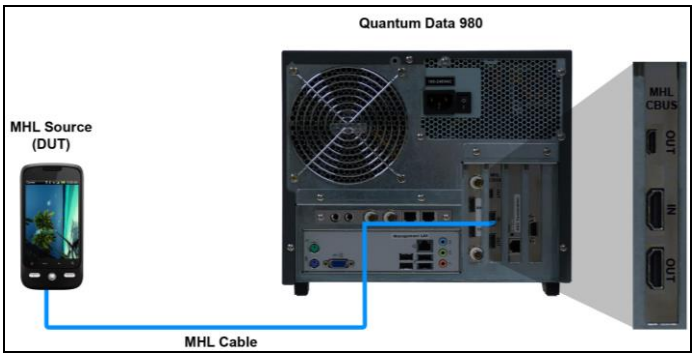
MHL Sink/Dongle Protocol Compliance Test Controller & CBUS Sink/Dongle Test suite
Purchase the MHL Sink/Dongle Protocol Compliance Test Controller (supported on HDMI Protocol Analyzer module and requires the 882EA) with the MHL CBUS sink/dongle compliance test suite.

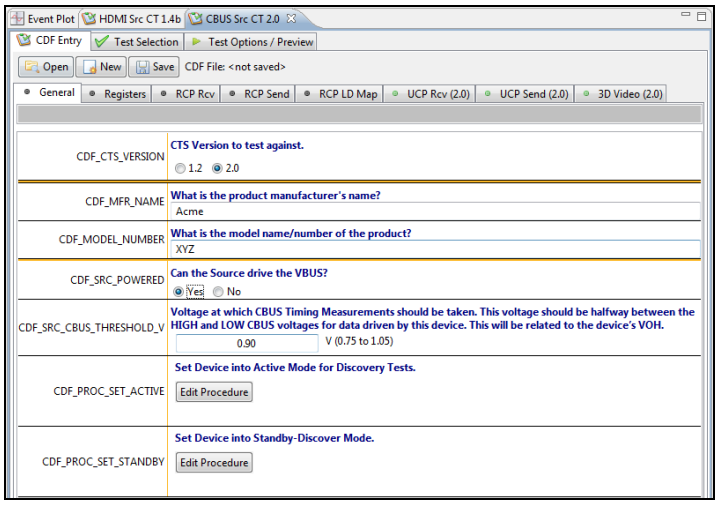
Rev. A8 – 07/19/2013

MHL CBUS SOURCE COMPLIANCE TESTING

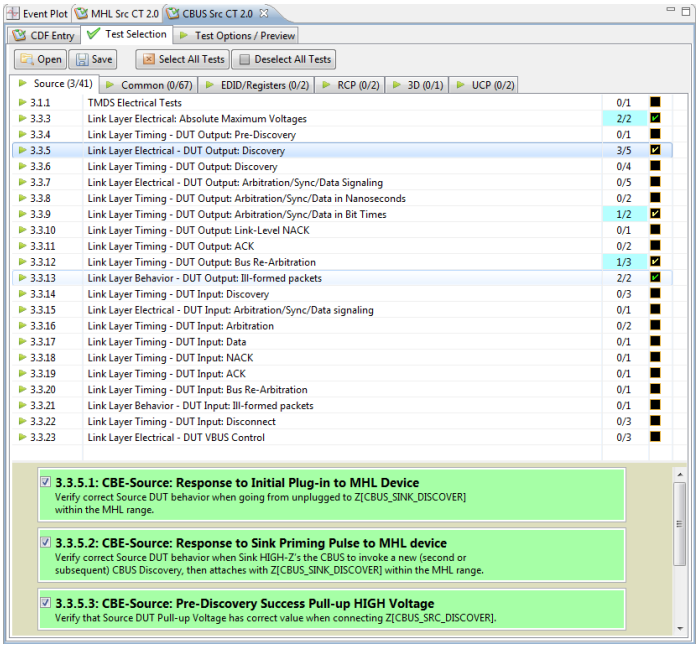
Operational workflow is simple:

1. Connect source device under test to 980.
2. Launch 980 GUI Manager.
3. Complete Capabilities Declaration Form (CDF).
4. Select the tests to run.
5. Review test suite and select options.
6. Initiate test series.
7. View Results.

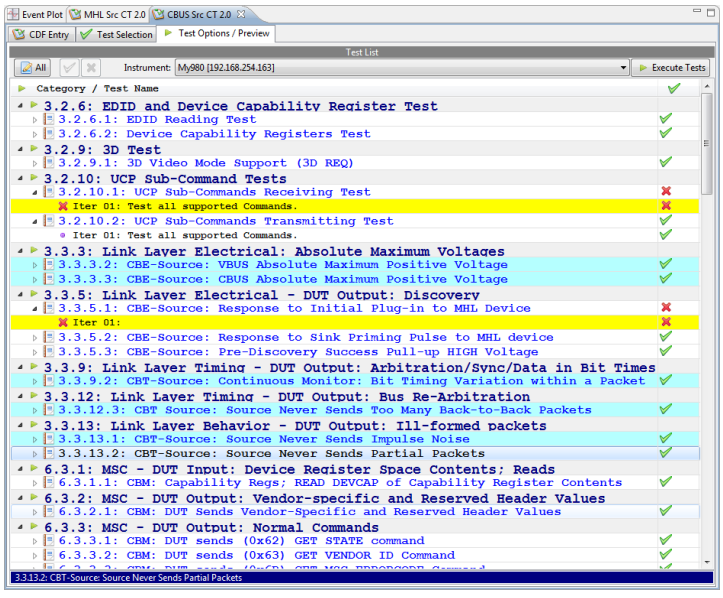




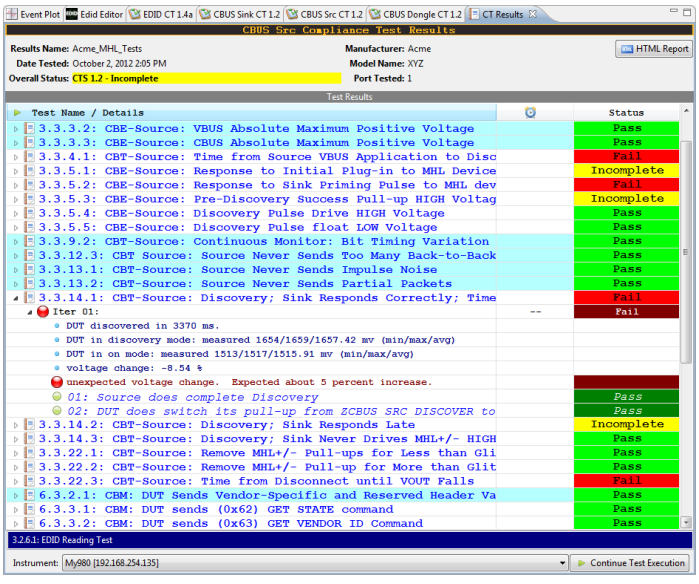
Capabilities Declaration Form (CDF) Registers page



Test Selections showing source test selections



MHL Source Compliance Test Preview



MHL Source Compliance Test Results

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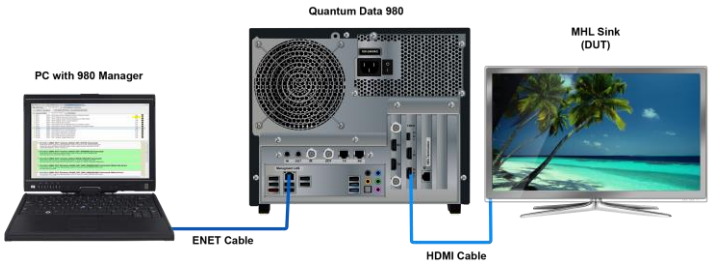
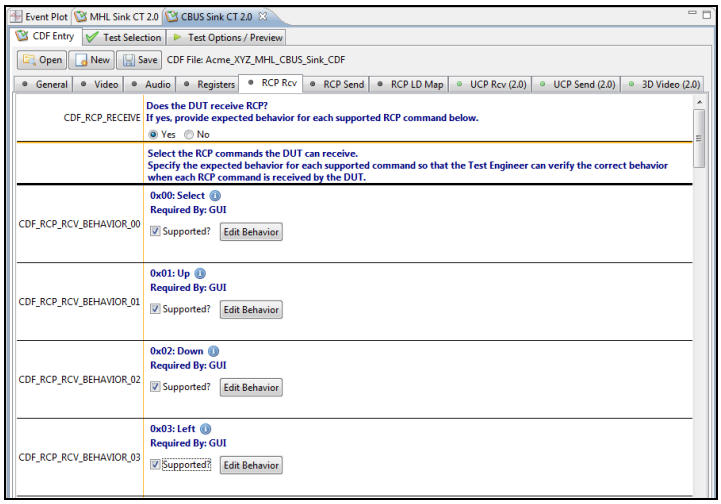
MHL CBUS SINK COMPLIANCE TESTING

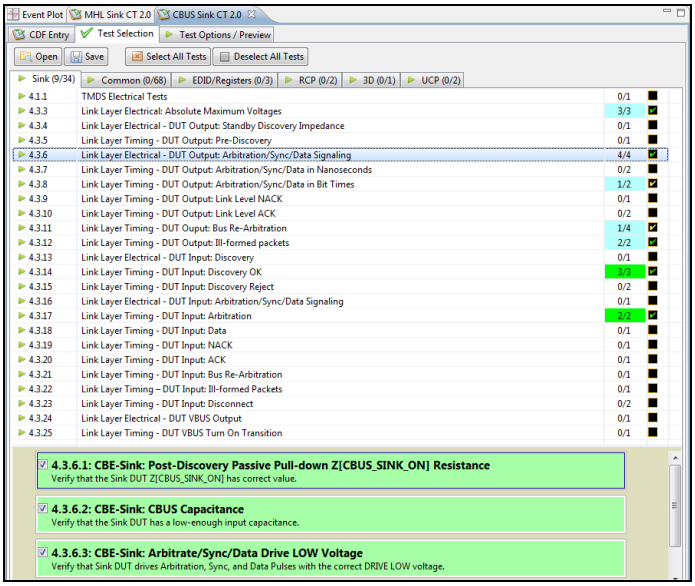
Operational workflow is simple:

1. Connect sink device under test to 980.
2. Launch 980 GUI Manager.
3. Complete Capabilities Declaration Form (CDF).
4. Select the tests to run.
5. Review test suite and select options.
6. Initiate test series.
7. View Results.

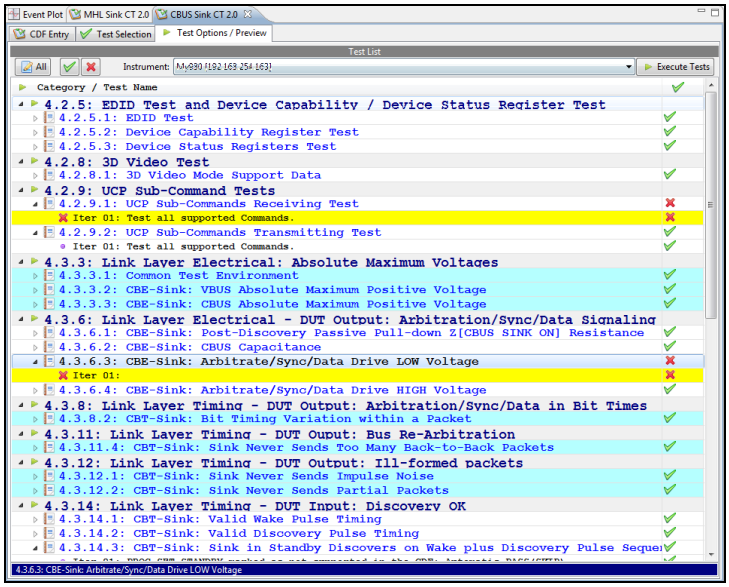




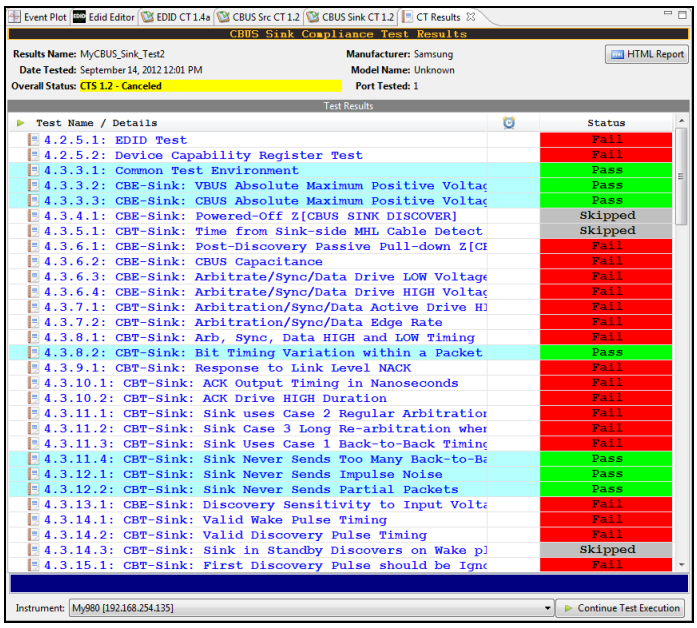
Capabilities Declaration Form (CDF) RCP page



Test Selections showing sink test selections



MHL Sink Compliance Test Preview



MHL Sink Compliance Test Results

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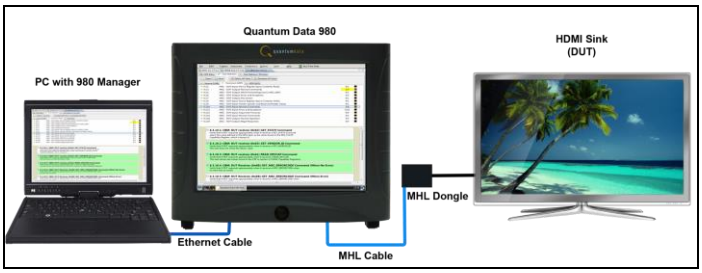
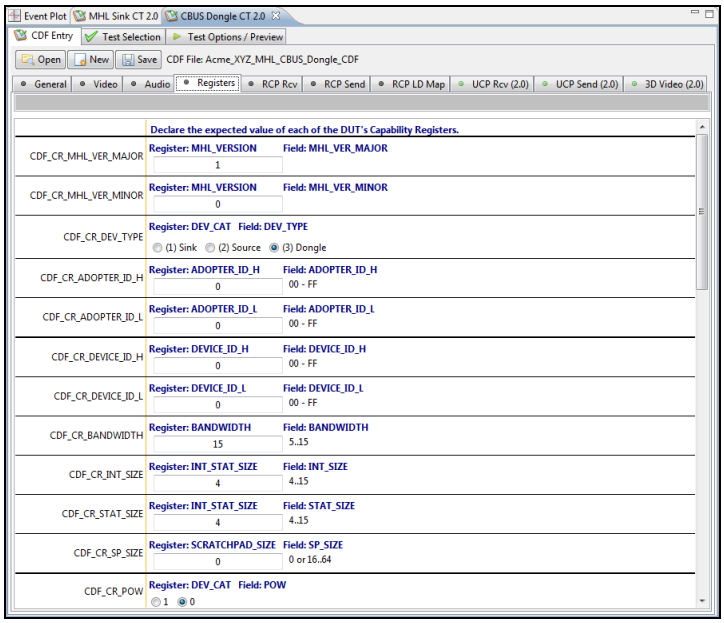
MHL CBUS DONGLE COMPLIANCE TESTING

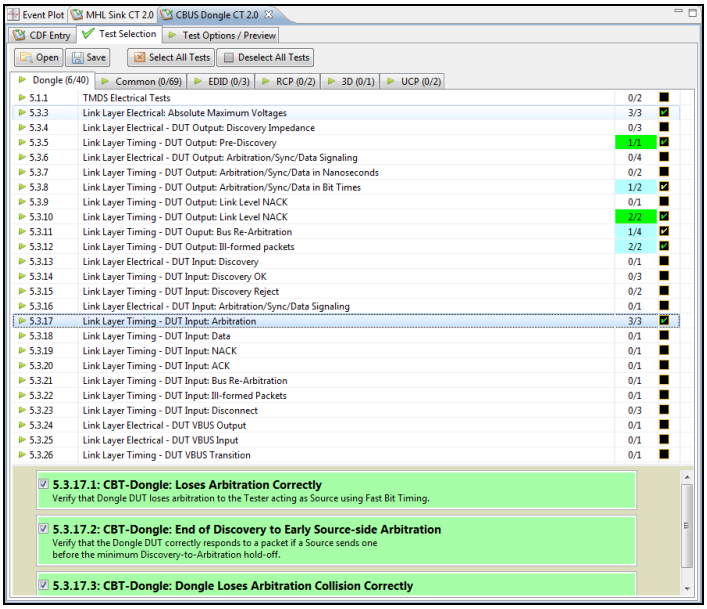
Operational workflow is simple:

1. Connect dongle device under test to 980.
2. Launch 980 GUI Manager.
3. Complete Capabilities Declaration Form (CDF).
4. Select the tests to run.
5. Review test suite and select options.
6. Initiate test series.
7. View Results.

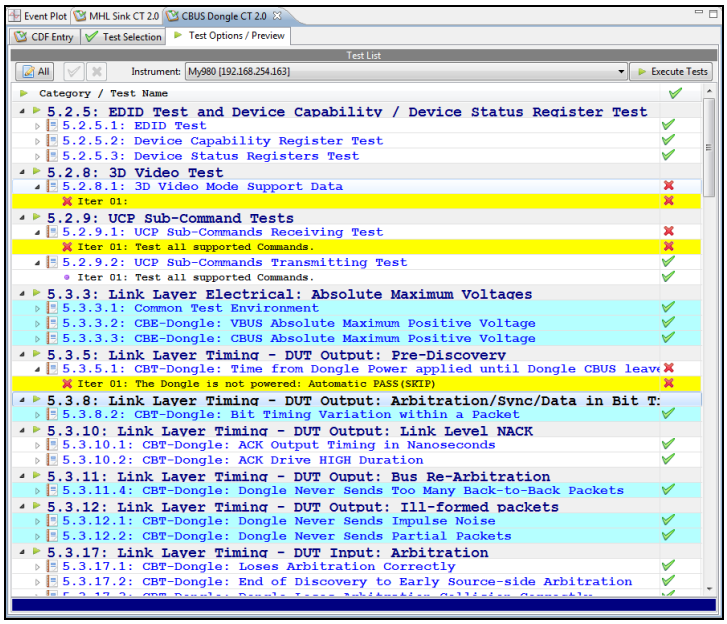




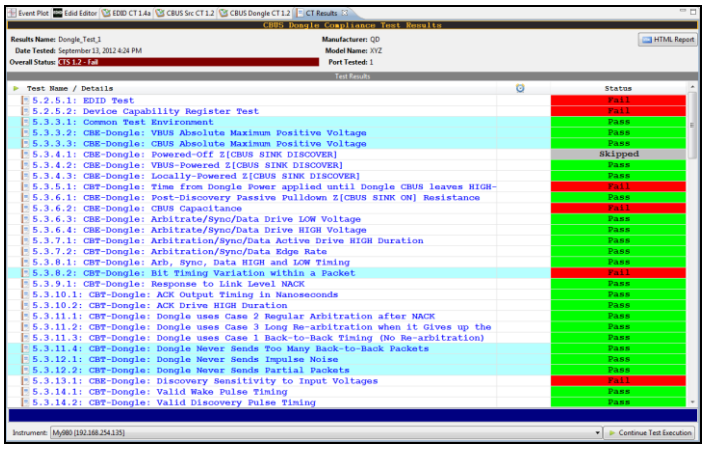
Capabilities Declaration Form (CDF) RCP page



Test Selections showing dongle test selections



MHL Dongle Compliance Test Preview



MHL Dongle Compliance Test Results

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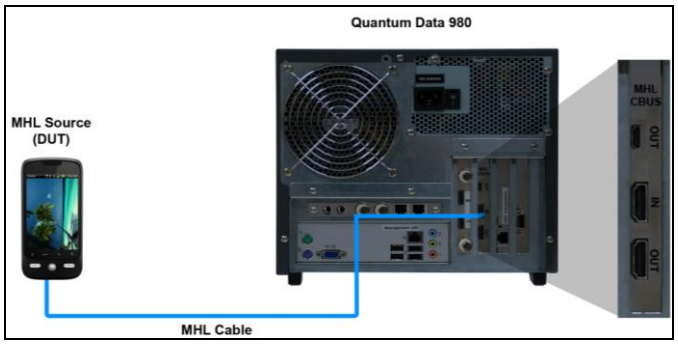
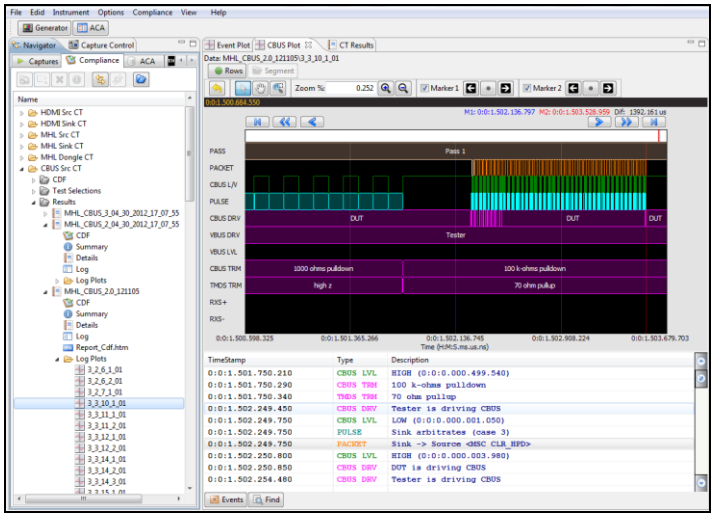
MHL CBUS EVENT LOG PLOTS

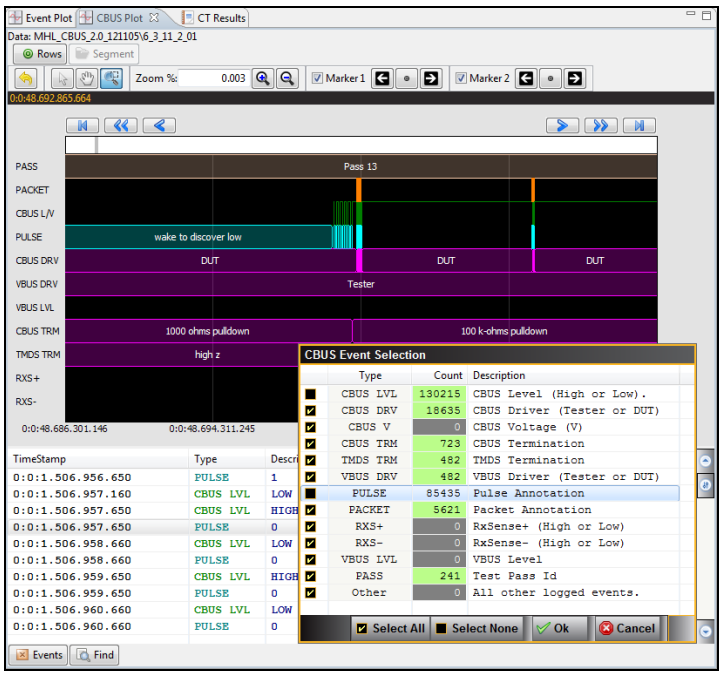
Provides graphical view of CBUS events:



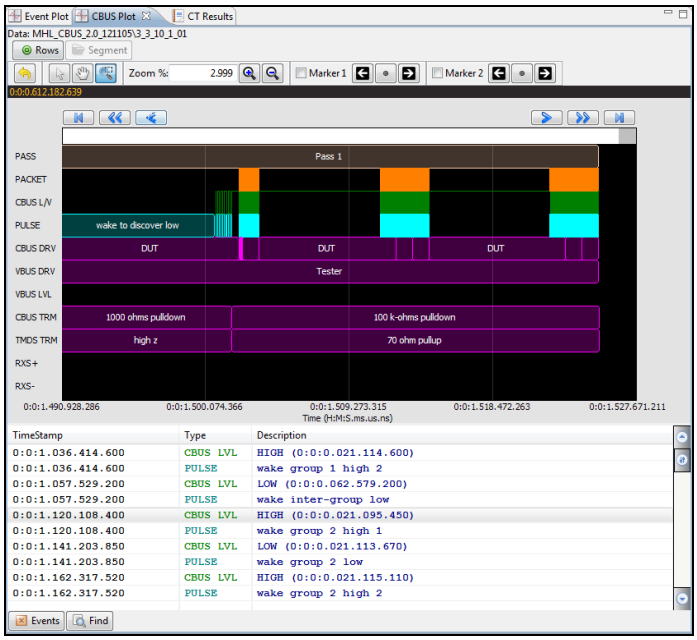
CBUS Source Test Setup (example)



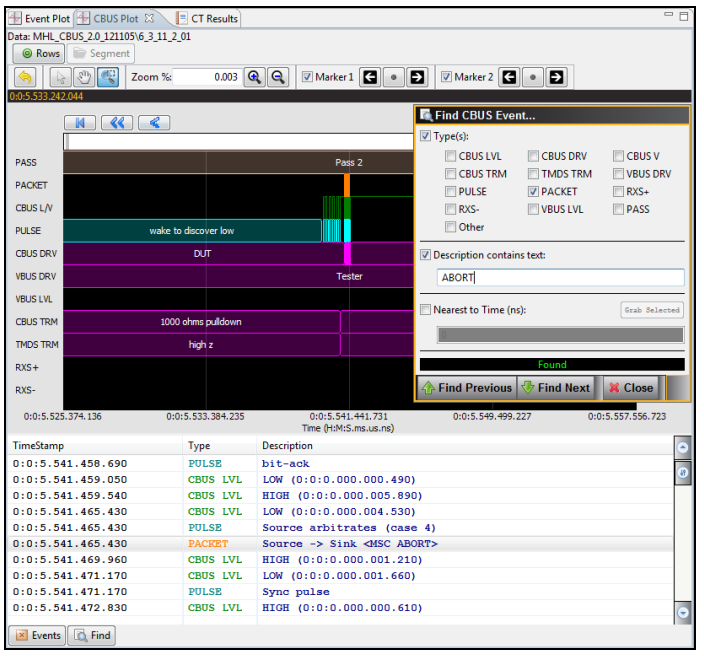
CBUS Log Plots Accessed via Navigator/Compliance Panel (right)



CBUS Log Plots (Filtering Events)



CBUS Log Plots (Source test example)



CBUS Log Plots (Searching for Events)

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MHL CBUS SOURCE COMPLIANCE TESTS

This module supports CBUS compliance testing of MHL source devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

3 Source Test

3.1 Electrical Test

3.1.1.13 Rx Sense Impedance

3.2 System Test

3.2.6 EDID and Device Capability Register Test
3.2.6.1 EDID Reading Test
3.2.6.2 Device Capability Registers Test (Available for MHL CTS 1.3, 2.0, 2.1)
3.2.7 RCP Sub-Command Tests
3.2.9 3D Video Tests (Available for MHL CTS 2.0, 2.1)
3.2.9.1 3D Video Mode Support (3D Req)
3.2.10 UCP Sub-Command Tests (Available for MHL CTS 2.0, 2.1)

3.3 CBUS Tests (all tests)

3.3.3 Link Layer Electrical – Source: Absolute Maximum Voltages
3.3.4 Link Layer Timing – Source DUT Output: Pre-Discovery
3.3.5 Link Layer Electrical – Source DUT Output: Discovery
3.3.6 Link Layer Timing – Source DUT Output: Discovery
3.3.7 Link Layer Electrical – Source DUT Output: Arbitration/Sync/Data Signaling
3.3.8 Link Layer Timing – Source DUT Output: Arbitration/Sync/Data in Nanoseconds
3.3.9 Link Layer Timing – Source DUT Output: Arbitration/Sync/Data in Bit Times
3.3.10 Link Layer Timing – Source DUT Output: Link-Level NACK
3.3.11 Link Layer Timing – Source DUT Output: ACK
3.3.12 Link Layer Timing – Source DUT Output: Bus Re-Arbitration
3.3.13 Link Layer Behavior – Source DUT Output: Ill-formed packets
3.3.14 Link Layer Timing – Source DUT Input: Discovery
3.3.15 Link Layer Electrical – Source DUT Input: Arbitration/Sync/Data signaling
3.3.16 Link Layer Timing – Source DUT Input: Arbitration
3.3.17 Link Layer Timing – Source DUT Input: Data
3.3.18 Link Layer Timing – Source DUT Input: NACK
3.3.19 Link Layer Timing – Source DUT Input: ACK
3.3.20 Link Layer Timing – Source DUT Input: Bus Re-Arbitration
3.3.21 Link Layer Behavior – Source DUT Input: Ill-formed packets
3.3.22 Link Layer Timing – Source DUT Input: Disconnect
3.3.23 Link Layer Electrical – Source DUT VBUS Control

MHL CTS Source tests supported by 980 HDMI Protocol Analyzer Module:

3.2.2 TMDS Encoding
3.2.2.1 Legal Codes
3.2.2.2 Basic Protocol
3.2.2.3 Packet Types
3.2.3 Video Modes
3.2.3.1 Video Formats
3.2.3.2 Pixel Encodings
3.2.3.3 AVI Infoframe
3.2.3.4 Video Quantization Ranges
3.2.4 Audio Tests
3.2.4.1 IEC 60958 / IEC61937
3.2.4.2 Audio Clock Regeneration
3.2.4.3 Audio Infoframes
3.2.5 EDID and Device Capability Register Test
3.2.5.1 Device Status Registers Test (Available for MHL CTS 2.0)
3.2.6 EDID and Device Capability Register Test
3.2.6.3 Device Status Registers Test (Available for MHL CTS 1.3, 2.0, 2.1)
3.2.8 RAP Sub-Command Tests (Available for MHL CTS 1.3, 2.0, 2.1)
3.2.9 3D Video Tests (Available for MHL CTS 2.0, 2.1)
3.2.9.2 3D Video Format Timings (Available for MHL CTS 2.0, 2.1)
3.2.9.3 3D Video Mode Indicator (Available for MHL CTS 2.0, 2.1)

MHL Source tests supported by 882EA Video Test Instrument:

3.2.5 HDCP Test

MHL CBUS SINK COMPLIANCE TESTS

This module supports CBUS compliance testing of MHL sink devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

4 MHL Sink Test

4.1 Electrical Test

4.1.1.7 Rx Sense Impedance

4.2 MHL System Tests (Requires 882EA except where noted)

4.2.5 EDID and Device Capability Register Test
4.2.5.1 EDID Test
4.2.5.2 Device Capability Registers Test
4.2.5.3 Device Status Registers Test (Available for MHL CTS 1.3, 2.0, 2.1)
4.2.6 RCP Sub-Command Test
4.2.8 3D Video Tests Available for MHL CTS 2.0, 2.1)
4.2.8.1 3D Video Mode Support Data
4.2.9 UCP Sub-Command Test (Available for MHL CTS 2.0, 2.1)

4.3 CBUS Tests (all tests)

4.3.3 Link Layer Electrical – Sink: Absolute Maximum Voltages
4.3.4 Link Layer Electrical – Sink DUT Output: Standby Discovery Impedance
4.3.5 Link Layer Timing – Sink DUT Output: Pre-Discovery
4.3.6 Link Layer Electrical – Sink DUT Output: Arbitration/Sync/Data Signaling
4.3.7 Link Layer Timing – Sink DUT Output: Arbitration/Sync/Data in Nanoseconds
4.3.8 Link Layer Timing – Sink DUT Output: Arbitration/Sync/Data in Bit Times
4.3.9 Link Layer Timing – Sink DUT Output: Link Level NACK
4.3.10 Link Layer Timing – Sink DUT Output: Link Level ACK
4.3.11 Link Layer Timing – Sink DUT Output: Bus Re-Arbitration
4.3.12 Link Layer Timing – Sink DUT Output: Ill-formed packets
4.3.13 Link Layer Electrical – Sink DUT Input: Discovery
4.3.14 Link Layer Timing – Sink DUT Input: Discovery OK
4.3.15 Link Layer Timing – Sink DUT Input: Discovery Reject
4.3.16 Link Layer Electrical – Sink DUT Input: Arbitration/Sync/Data Signaling
4.3.17 Link Layer Timing – Sink DUT Input: Arbitration
4.3.18 Link Layer Timing – Sink DUT Input: Data
4.3.19 Link Layer Timing – Sink DUT Input: NACK
4.3.20 Link Layer Timing – Sink DUT Input: ACK
4.3.21 Link Layer Timing – Sink DUT Input: Bus Re-Arbitration
4.3.22 Link Layer Timing – Sink DUT Input: Ill-formed Packets
4.3.23 Link Layer Timing – Sink DUT Input: Disconnect
4.3.24 Link Layer Electrical – Sink DUT VBUS Output
4.3.25 Link Layer Timing – Sink DUT VBUS Turn On Transition

MHL CTS Sink tests supported by 980 HDMI Protocol Analyzer Module:

4.2 MHL System Tests (Requires 882EA except where noted)

4.2.1 TMDS Coding (Requires 882EA except where noted)
4.2.1.1 Character Synchronization (882EA not required)
4.2.1.2 Packet Type
4.2.2 Video Tests (Requires 882EA)
4.2.2.1 Video Format
4.2.2.2 Pixel Encoding
4.2.2.3 Video Quantization Ranges
4.2.3 Audio Test (Requires 882EA)
4.2.3.1 IEC 60958 / IEC 61937
4.2.3.2 Audio Clock Regeneration
4.2.7 RAP Sub-Command Test (Available for MHL CTS 2.0, 2.1)
4.2.8 3D Video Tests (Available for MHL CTS 2.0, 2.1)
4.2.8.2 3D Video Format (Available for MHL CTS 2.0, 2.1)

MHL Sink tests supported by 882EA Video Test Instrument:

4.2.4 HDCP Test

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MHL CBUS DONGLE COMPLIANCE TESTS

This module supports CBUS compliance testing of MHL sink devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

5 MHL Dongle Test
5.1 Electrical Test
5.1.1.7 Rx Sense Impedance (Powered)
5.1.1.8 Rx Sense Impedance (Unpowered)

5.2 MHL System Tests (Requires 882EA except where noted)
5.2.5 EDID and Device Capability Register Test
5.2.5.1 EDID Test
5.2.5.2 Device Capability Registers Test
5.2.5.3 Device Status Registers Test (Available for MHL CTS 1.3,2.0, 2.1)
5.2.6 RCP Sub-Command Test
5.2.8 3D Video Tests (Available for MHL CTS 2.0, 2.1)
5.2.8.1 3D Video Mode Support Data
5.2.9 UCP Sub-Command Test (Available for MHL CTS 2.0, 2.1)

5.3 CBUS Tests (all tests)
5.3.3 Link Layer Electrical – Dongle: Absolute Maximum Voltages
5.3.4 Link Layer Electrical – Dongle DUT Output: Discovery Impedance
5.3.5 Link Layer Timing – Dongle DUT Output: Pre-Discovery
5.3.6 Link Layer Electrical – Dongle DUT Output: Arbitration/Sync/Data Signaling
5.3.7 Link Layer Timing – Dongle DUT Output: Arbitration/Sync/Data in Nanoseconds
5.3.8 Link Layer Timing – Dongle DUT Output: Arbitration/Sync/Data in Bit Times
5.3.9 Link Layer Timing – Dongle DUT Output: Link Level NACK
5.3.10 Link Layer Timing – Dongle DUT Output: Link Level ACK
5.3.11 Link Layer Timing – Dongle DUT Output: Bus Re-Arbitration
5.3.12 Link Layer Timing – Dongle DUT Output: Ill-formed packets
5.3.13 Link Layer Electrical – Dongle DUT Input: Discovery
5.3.14 Link Layer Timing – Dongle DUT Input: Discovery OK
5.3.15 Link Layer Timing – Dongle DUT Input: Discovery Reject
5.3.16 Link Layer Electrical – Dongle DUT Input: Arbitration/Sync/Data Signaling
5.3.17 Link Layer Timing – Dongle DUT Input: Arbitration
5.3.18 Link Layer Timing – Dongle DUT Input: Data
5.3.19 Link Layer Timing – Dongle DUT Input: NACK
5.3.20 Link Layer Timing – Dongle DUT Input: ACK
5.3.21 Link Layer Timing – Dongle DUT Input: Bus Re-Arbitration
5.3.22 Link Layer Timing – Dongle DUT Input: Ill-formed Packets
5.3.23 Link Layer Timing – Dongle DUT Input: Disconnect
5.3.24 Link Layer Electrical – Dongle DUT VBUS Output
5.3.25 Link Layer Electrical – Dongle DUT VBUS Input
5.3.26 Link Layer Timing – Dongle DUT VBUS Transition

MHL CTS Dongle tests supported by 980 HDMI Protocol Analyzer Module:
5.2.1 TMDS Coding (Requires 882EA except where noted)
5.2.1.1 Character Synchronization (882EA not required)
5.2.1.2 Packet Type
5.2.2 Video Tests (Requires 882EA)
5.2.2.1 Video Format
5.2.2.2 Pixel Encoding
5.2.2.3 Video Quantization Ranges
5.2.3 Audio Test (Requires 882EA)
5.2.3.1 IEC 60958 / IEC 61937
5.2.3.2 Audio Clock Regeneration
5.2.7 RAP Sub-Command Test (Available for MHL CTS 2.0, 2.1)
5.2.8 3D Video Tests (Available for MHL CTS 2.0, 2.1)
5.2.8.2 3D Video Format

MHL Dongle tests supported by 882EA Video Test Instrument:
5.2.4 HDCP Test (supported through 882EA)

MHL CBUS COMMON COMPLIANCE TESTS

This module Supports CBUS compliance common tests for MHL Common devices in accordance with MHL CTS 1.2, 1.3, 2.0 & 2.1.

6 Tests Common to Sources, Sinks, Dongles
6.3 CBUS Tests (all tests)
6.3.1 MSC – Source and Sink DUT Input: Device Register Space Contents; Reads
6.3.2 MSC – Source and Sink DUT Output: Vendor Specific and Reserved Header Values
6.3.3 MSC – Source and Sink DUT Output: Normal Commands
6.3.4 MSC – Source and Sink DUT Output: NACK Packet Response to MSC_MSG
6.3.5 MSC – Source and Sink DUT Output: Never Initiates Bad Commands
6.3.6 MSC – Source and Sink DUT Output: Errors and Exceptions
6.3.7 MSC – Source and Sink DUT Output; Disconnect
6.3.8 MSC – Source and Sink DUT Input: Device Register Space Contents; Writes
6.3.9 MSC – Source and Sink DUT Input: Vendor Specific and Reserved Header Values
6.3.10 MSC – Source and Sink DUT Input: Normal Commands
6.3.11 MSC – Source and Sink DUT Input: Errors and Exceptions
6.3.12 MSC – Source and Sink DUT Input: Argument Timeouts
6.3.13 MSC – Source DUT Output: Never Initiates Bad Commands
6.3.14 MSC – Source DUT Input: Normal Commands
6.3.15 MSC – Sink DUT Output: Normal Commands
6.3.16 MSC – Sink DUT Input: Errors and Exceptions
6.3.17 DDC – Source DUT Output; DUT Never Sends Illegal DDC Command
6.3.18 DDC – Source DUT Output; Normal Operation
6.3.19 DDC – Source DUT Output; Illegal Responses
6.3.20 DDC – Sink DUT Input; Continuous Monitors and Normal Operation
6.3.21 DDC – Sink DUT Input; Normal Operation
6.3.22 DDC – Sink DUT Input; Illegal Responses